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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/160,824	09/25/1998	TSIU CHAN	97-C-108	6763

30425 7590 01/24/2003

STMICROELECTRONICS, INC.
MAIL STATION 2346
1310 ELECTRONICS DRIVE
CARROLLTON, TX 75006

EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 01/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/160,824	[redacted]AN ET AL.	
	Examiner	Art Unit	
	Thomas L Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,9-16,18 and 19* is/are rejected.

7)☒ Claim(s) *7,8 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 September 1998* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restriction

1. Applicant's election without traverse of Group I, claims 1-19 in Paper No. 4 is acknowledged.

Oath/Declaration

2. The oath/declaration filed on 09/25/98 is acceptable.

Drawings

3. The drawings are objected to by the PTO Draftsperson for the reasons noted on the Notice of Draftsperson's Patent Drawing Review, form PTO-948, attached to paper #5.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, in claims 12 and 19, the first and second chip "profiles" and the relationship of said "profiles" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Priority

4. Applicants have made no claim for priority.

Claim Rejections - 35 USC § 112

In paper #12, Applicant points out that claims 7 and 9 do not claim connections to some undisclosed external computer, but rather these claims merely claim the ordinary sort of I/O pads seen as part 20 figure 2 of the instant application, or part 403 of the "conventional" microprocessor of figure 4A of KANEKO 6,255,736, or part 13 of the invention shown in figure 5A of KANEKO, or part 208 of the invention shown in figure 14 of WENZEL et al., 6,150,724. Because these claims claim an additional feature that one having skill in the art would readily understand the scope of, the rejection of claims 7 and 9 under the first paragraph of § 112 is withdrawn.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

A. Claims 1,3,6,9,11,12,13,14, and 19 rejected under 35 U.S.C. 102(e) as being anticipated by KANEKO (6,255,736).

Kaneko discloses a microprocessor comprising a first chip, or integrated circuit chip 11, having an active face including a central processing unit 41; and a second chip, or integrated circuit chip 12, having an active face, the second chip 12 mounted on, and electrically connected to, the active face of the first chip, further comprising at least one

metal region 20 projecting from the active face of the first integrated circuit chip 11, at least one metal region 21 projecting from a surface of the second integrated circuit chip 12, the metal regions further comprising: conductive regions projecting from the active faces of the first 11 and second 12 chips (note that only one alternate structure of claim 14 need be present), and at least two groups of contact pads 13 on the active surface of the first integrated circuit chip 11 for external connection to the central processing unit 41, wherein the second chip 12, or integrated circuit chip 12, adds functionality, or provides added functionality, to the central processing unit 41 of the first chip 11, wherein the electrical connection is by a bonding layer 20A between the metal regions 20 and 21 on the active faces of the first 11 and second 12 chips, wherein an active face of the second integrated circuit chip 12 faces the active face of the first integrated circuit chip 11, wherein the at least one metal region 20 projecting from the active face of the first integrated circuit chip 11 overlies the at least one metal region 21 projecting from a surface of the second integrated circuit chip 12, wherein the electrical connection between the first integrated circuit chip 11 and the second integrated circuit chip 12 is by direct connection of metal regions 20 and 21 on the active faces of the first 11 and second 12 integrated circuit chips by a bonding layer 20A, wherein a length and width of the second integrated circuit chip 12 are less than a respective length and width of the first integrated circuit chip 11, and wherein a width of the second integrated circuit chip 12 is less than a width of the first integrated circuit chip 11, and is less than a distance between the two groups of contact pads 13, and wherein the active regions of the first

11 and second 12 chips are spaced apart by the metal regions 20 and 21. Note figures 5A, 5B, and 7 and column 6 lines 60-67, column 7 line 66-67, and column 8 lines 1-9 of Kaneko

B. Claims 1-6,9-11,13,15,16,18, and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by WENZEL et al. (6,150,724).

Wenzel et al. discloses a microprocessor comprising a first chip 102, or integrated circuit chip, having an active face including a central processing unit; and a second chip 104, or integrated circuit chip, having an active face, the second chip 104 mounted on, and electrically connected to, the active face of the first chip 102, further comprising a third chip (not shown, see figure 8 and column 6 lines 47-59) or integrated circuit chip mounted on, and electrically connected to, the active face of the first chip 102 or integrated circuit chip adjacent the second chip 104 and at least two groups of contact pads 208 on the active surface of the first integrated circuit chip 102 for external connection to the central processing unit, wherein the second chip 104, or integrated circuit chip, adds functionality, or provides added functionality, to the central processing unit of the first chip 102 and the third chip adds further functionality to the central processing unit of the first chip 102 or integrated circuit, wherein the electrical connection is by a bonding layer 312 between metal regions 210 and 310 projecting from the active faces of the first 102 and second 104 chips, wherein the electrical connection between the first integrated circuit chip 102 and the second integrated circuit chip 104 is by direct connection of the metal regions 210 and 310 projecting from the

active faces of the first 102 and second 104 integrated circuit chips by a bonding layer 312, wherein an active face of the second integrated circuit chip 104 faces the active face of the first integrated circuit chip 102, wherein the metal region 210 projecting from the active face of the first integrated circuit chip 102 overlies the metal region 310 projecting from a surface of the second integrated circuit chip 104, wherein the second integrated circuit chip 104 has a width less than a distance between the two groups of contact pads 208, and wherein a width of the second integrated circuit chip 104 is less than a width of the first integrated circuit chip 102, and wherein the central processing unit comprises one of a digital signal processor and a field programmable gate array, and the second integrated circuit chip 104 comprises one of a cache memory, a dynamic random access memory (DRAM), a static random access memory (SRAM), and a flash memory, and an analog-to-digital converter.

Note figures 5 and 14 and column 6 lines 47-53 and 60-67 and column 7 lines 1-17 of Wenzel et al. With respect to the CPU/DSP/A-D/cache/DRAM/SRAM/flash limitations, note that in column 6 spanning to column 7, Wenzel et al. state that

> Generally, the structure of FIG. 5 may be used to integrate any one integrated circuit device with one or more other integrated circuit device(s) either made by the same process or different processes. For example, one of either the chip 102 or chip 104 may be a digital signal processor (DSP), a microcontroller (MCU), a general purpose microprocessor or computer central processing unit (CPU), an analog-to-digital (A/D) converter, a digital-to-analog (D/A) converter, any memory device (such as a DRAM, an static random access memory (SRAM), an electrically programmable read only memory (EPROM), an EEPROM, a ferroelectric memory, a nonvolatile memory, a read only memory (ROM), ferromagnetic memory, optical storage, or the like), bipolar device, power metal on semiconductor field effect transistor (MOSFET) devices, radio frequency (RF) devices, infrared (IF) devices, analog or digital devices, sensors, discrete devices, micromachined devices, application specific integrated circuits (ASICs), telecommunications ICs, III-V devices, oscillators, liquid crystal display (LCD) displays, **or any other device typically made in integrated circuit or electrical circuit form, while the other device 102 or 104 may be any one of the same**. In a preferred form, one of the devices 102 or 104 will be some execution unit, such as a microprocessor CPU, while the other device of 102

or 104 will be some memory structure which functions as local memory for the CPU (e.g., a cache or embedded memory).

Allowable Subject Matter

6. Claims 7,8,and 17 are objected to as being dependent upon rejected base claims, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments filed 11/18/02 have been fully considered. Applicant's arguments concerning the § 112 rejections of claims 7 and 9 are considered well founded. Applicant's arguments with respect to claims 1-6,9-16,18, and 19 are moot in view of the new ground(s) of rejection.

Conclusion

8. Papers related to this application may be submitted to Technology Center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 3-C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2826 Fax Center number is (703) 308-7722 and 308-7724. The Group 2800 Fax Center is to be used only for papers related to Group 2800 applications.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TLD
01/2003

Minh Loan Tran
Primary Examiner